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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,695	07/24/2003	Kazuhiro Nakajima	8053-1016	9942

466 7590 12/14/2005

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,695	NAKAJIMA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/26/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 30 is objected to because of the following informalities: Claim 30 recites the limitation "said at least one first metal wiring layer" in line 16-17. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 30 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of one first metal wiring layer, as recited in claim 30, is unclear as to the structural relationship between the one first metal wiring layer is the previously recited "one first metal wiring pattern layer".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 and 24-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shea et al. (6,694,208) in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 1, 24, and 29-30, Shea et al. teach in related text (column 1, lines 20-25 and column 2, lines 57-65) a production process for producing plurality of a semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first metal wiring layer on each of said chip areas;

subjecting said wafer to a provisional yield-rate test in which it is examined whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable; and

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device when said wafer passes said provisional yield-rate test.

Shea et al. do not explicitly state that the further processing of said wafer include forming a second metal wiring layer on said first metal wiring layer.

AAPA teaches in figures 16 and 17 and related text (pages 1-5 and 35-38) further processing of said wafer includes forming a second metal wiring layer 48' on a first metal wiring layer 16'.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to further process said wafer of Shea et al. by forming a second

metal wiring layer on said first metal wiring layer in order to obtain operational device by providing electrical connections to the device.

Regarding claim 2, 5-6 and 25, Shea et al. teach that a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and it is determined that said wafer has passed said provision yield-rate test when said yield-rate exceeds a predetermined permissible rate,

subjecting said wafer to a genuine yield-rate test which it is examined whether each of the finished semiconductor devices on said wafer is acceptable or unacceptable thereby find a yield-rate of acceptable finished semiconductor devices; and finally processing said wafer when said wafer passes said genuine yield-rate test,

wherein a yield-rate of acceptable finished semiconductor devices is found in said genuine yield-rate test, and it is determined that said wafer has passed said genuine yield-rate test when said yield-rate exceeds a predetermined permissible rate, wherein said customized wiring-arrangement section has a plurality of electrode pads formed on an uppermost surface thereof, and said genuine yield-rate test is carried out, using the electrode pads of said customized wiring-arrangement section,

Regarding claims 3-4, 7-8 and 26-28, AAPA teaches first metal wiring layer is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and second metal wiring layer is formed as a customized wiring-arrangement section to establish electrical interconnections among

said basic electrical component formation areas in accordance with a customer's request,

wherein said basic wiring-arrangement section has a plurality of electrode pads 58' formed an uppermost surface thereof, for carrying out said provisional yield-rate test,

wherein said basic wiring-arrangement section is formed as a multi-layered wiring-arrangement section 16' (see figure 16) composed at least two metal circuit pattern layers 36', 40' and at least one insulation layer 38' alternately laminated on each of said chip areas, and said customized wiring-arrangement section 48' is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer 54 alternately laminated on said basic wiring-arrangement section.

Regarding claims 24 and 29, Shea et al. teach first and second test sections (column 2, line 2-17).

Regarding claim 29, the claimed limitations of first and second test sections electrically connected to an active region of said chip area are inherent in prior art's device because the first and second test sections test the metal layers which in turn must be electrically connected to an active region of said chip area.

Response to Arguments

Applicant's arguments with respect to claims 1-8 and 24-30 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
12/7/05

ORI NADAV
PRIMARY EXAMINER
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